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## **CLAIMS**

What is claimed is:

5 \ \ \ 1. A method for forming a pocket dopant region of an indium ion, the method comprising:

providing a P-type semiconductor substrate;

forming a dielectric layer on said P-type semiconductor substrate; forming and defining a photoresister layer on said dielectric layer; performing a N-type ion-implanting process by way of using said photoresister layer as an ion-implanting mask to form a N-type ion-implanting region in said P-type semiconductor substrate; and

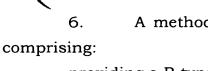
performing a pocketed ion-implantation with an indium ion by way of using said photoresister layer as said ion-implanting mask to form said pocket dopant region of said indium ion closed to beside said N-type ion-implanting region.

- 2. The method according to claim 1, wherein said dielectric layer comprises a stack dielectric layer.
- 3. The method according to claim 2, wherein said stack dielectric layer comprises a oxide-nitride-oxide layer.
- 4. The method according to claim 1, wherein the method for forming said dielectric layer comprises a depositing process.
  - 5. The method according to claim 1, wherein said N-type ion-implanting region comprises a source/drain region.

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A method for forming a read only memory, the method

providing a P-type semiconductor substrate;

forming a dielectric layer on said P-type semiconductor substrate; forming and defining a plurality of photoresister layers on said dielectric layer to expose a portion of said dielectric layer;

performing a pocketed ion-implantation with an indium ion at least one time by way of using said plurality of photoresister layers as a plurality of ion-implanting masks to form a plurality of pocket dopant regions having said indium ion in said P-type semiconductor substrate; and

performing a N-type ion-implanting process by way of using said plurality of photoresister layers as said ion-implanting masks to form a plurality of N-type ion-implanting regions in said P-type semiconductor substrate between said plurality of photoresist layers; and

removing said plurality of photoresist layers to form said read only memory.

- 7. The method according to claim 6, wherein said dielectric layer comprises an nitride layer.
  - 8. The method according to claim 6, wherein the method for forming said dielectric layer comprises a depositing process.
- 25 9. The method according to claim 6, wherein said plurality of pocket dopant regions having said indium ion are located in said P-type semiconductor substrate beside said plurality of N-type ion-implanting regions.

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- 10. The method according to claim 6, wherein said plurality of N-type ion-implanting regions comprises a plurality of source/drain regions.
- 11. A method for forming a read only memory, the method comprising:

providing a P-type semiconductor substrate;

forming a dielectric layer on said P-type semiconductor substrate; forming and defining a plurality of photoresister layers on said dielectric layer to expose a portion of said dielectric layer;

performing an etching process by way of using said plurality of photoresister layers as a plurality of etching masks to etch said dielectric layer and form a plurality of memory cells;

performing a pocketed ion-implantation with an indium ion at least two time by way of using said plurality of photoresister layers as a plurality of ion-implanting masks to form a plurality of pocket dopant regions having said indium ion beside said P-type semiconductor substrate under said plurality of memory cells; and

performing a N-type ion-implanting process by way of using said plurality of photoresister layers as said ion-implanting masks to form a plurality of N-type ion-implanting regions in said P-type semiconductor substrate between said plurality of memory cells; and

removing said plurality of photoresist layers to form said read only memory.

12. The method according to claim 11, wherein said dielectric layer comprises an nitride layer.

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- 13. The method according to claim 11, wherein the method for forming said dielectric layer comprises a depositing process.
- The method according to claim 11, wherein said plurality of pocket dopant regions having said indium ion are located in said P-type semiconductor substrate beside said plurality of N-type ion-implanting regions.
- 15. The method according to claim 11, wherein said plurality of N-type ion-implanting regions comprises a plurality of source/drain regions.
  - 16. A method for forming an nitride read only memory, the method comprising:

providing a P-type semiconductor substrate;

forming an oxide-nitride-oxide layer on said P-type semiconductor substrate;

forming and defining a plurality of photoresister layers on said oxide-nitride-oxide layer to expose a portion of said oxide-nitride-oxide layer;

performing an etching process by way of using said plurality of photoresister layers as a plurality of etching masks to etch said oxidenitride-oxide layer and form a plurality of read only memory cells;

performing a N-type ion-implanting process by way of using said plurality of photoresister layers as an ion-implanting masks to form a plurality of N-type ion-implanting regions in said P-type semiconductor substrate between said plurality of read only memory cells;

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performing a pocketed ion-implantation with an indium ion at least two time by way of using said plurality of photoresister layers as said plurality of ion-implanting masks to form a plurality of pocket dopant regions having said indium ion beside said P-type semiconductor substrate under said plurality of memory cells; and

removing said plurality of photoresist layers to form said nitride read only memory.

17. The method according to claim 16, wherein the method for forming said oxide-nitride-oxide layer comprises a depositing process.

- 18. The method according to claim 16, wherein said plurality of N-type ion-implanting regions are separated by a channel from each other.
- 19. The method according to claim 16, wherein said plurality of N-type ion-implanting regions comprises a plurality of source/drain regions.
- 20. The method according to claim 16, wherein said plurality of pocket dopant regions having said indium ion are located in said P-type semiconductor substrate beside said plurality of N-type ion-implanting regions.

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